3.125 Gbps 4x4 LVDS Crosspoint Switch with Transmit Pre-emphasis and Receive Equalization

DS25CP104 Evaluation Kit

USER MANUAL

Part Number: DS25CP104EVK

For the latest documents concerning these products and evaluation kit, visit lvds.national.com.
Schematics and gerber files are also available at lvds.national.com.

June 2007
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Overview

The DS25CP104EVK is an evaluation kit designed for demonstrating performance of DS25CP104, a 3.125 Gbps 4x4 LVDS Crosspoint Switch with Transmit Pre-emphasis and Receive Equalization. The evaluation kit is comprised of the DS25CP104 with its associated input and output SMA connectors and jumpers to manually select the desired pre-emphasis or equalization. The kit also includes an integrated USB to SMBus conversion circuit to control the SMBus with a PC, and three FR4 striplines (15" (38.1cm), 30" (76.2cm), and 60" (152.4cm)) to exercise the devices' signal conditioning features (pre-emphasis and equalization).

The purpose of this document is to familiarize the user with the DS25CP104EVK, to suggest test setup procedures and instrumentation to test the device optimally, and to guide the user through some typical measurements that demonstrate the performance of the DS25CP104 in typical applications.

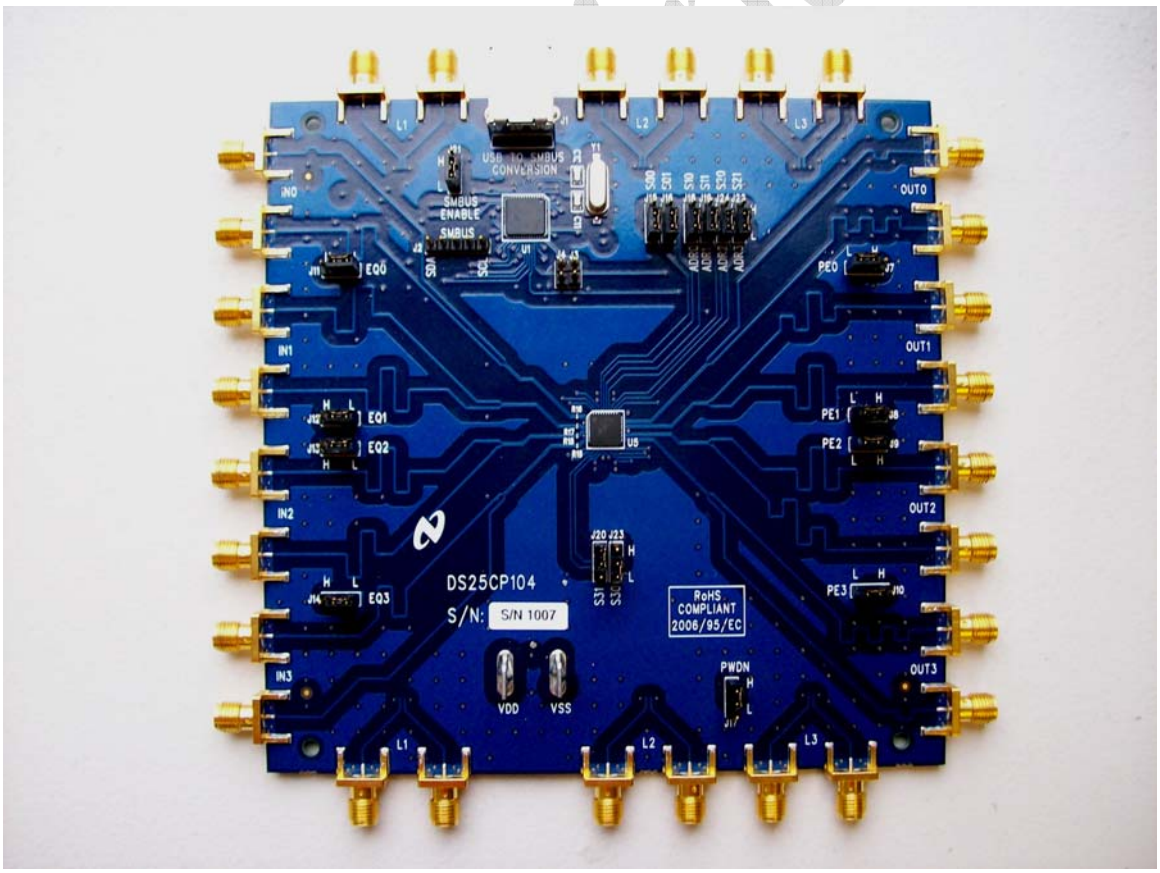


Figure 1. Photo of the DS25CP104EVK

DS25CP104EVK Description

Figure 2 shows the top layer drawing of the PCB with the silkscreen annotations. The 4.5 by 4.5 inch, eight-layer PCB is designed to evaluate the functions of the DS25CP104.

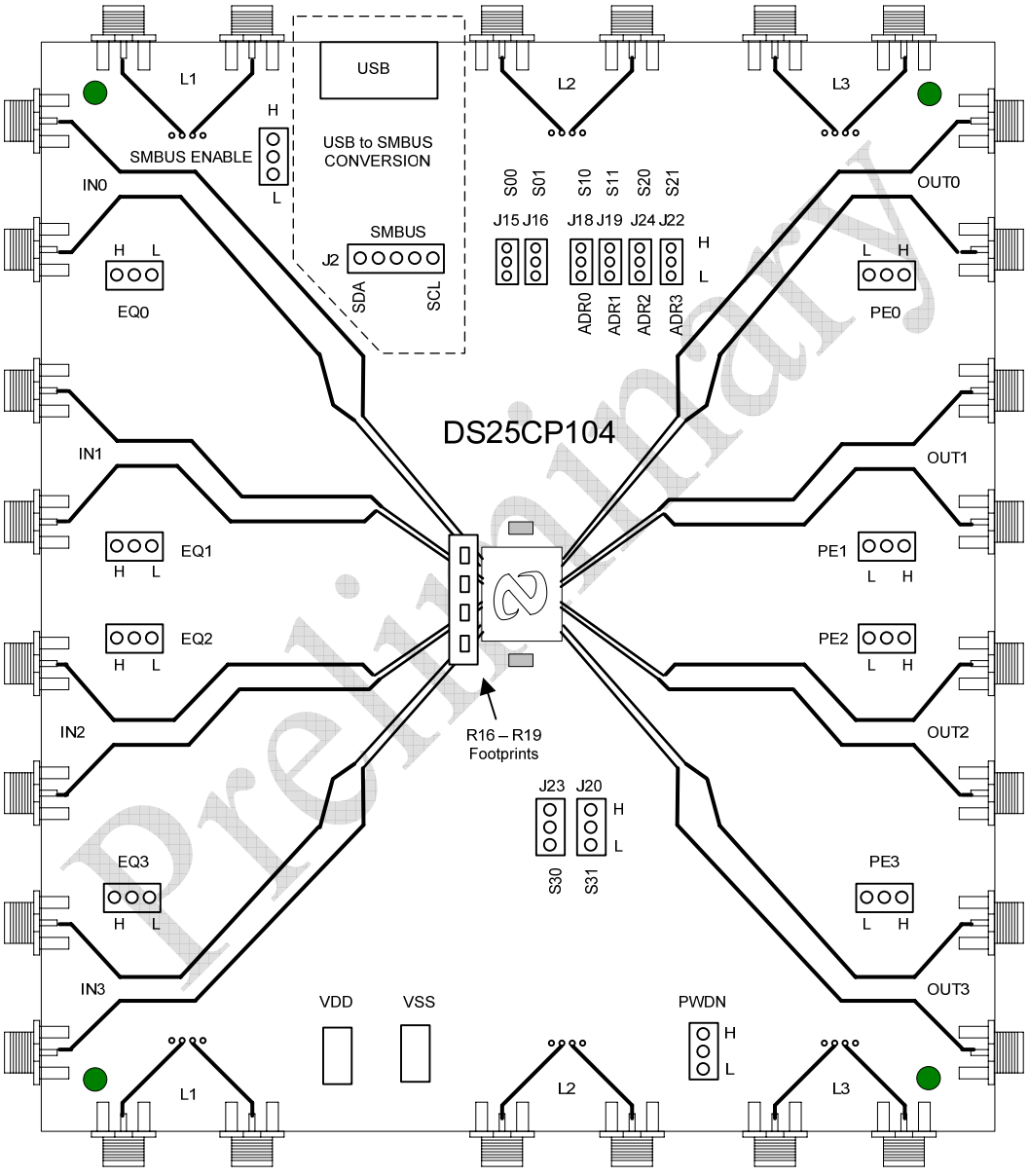


Figure 2. Top Layer DS25CP104EVK

For descriptive purposes the DS25CP104EVK can be broken into three parts:

1. The **DS25CP104** IC with associated connectors and jumpers is the main part of the board. The block diagram of the DS25CP104 is shown in Figure 3. The receive buffers can be set to Off and Low equalization by the external pins EQ0 – EQ3; the transmit buffers has can be set to Off and Med. levels of pre-emphasis by the external pins PE0 – PE3. Since data capabilities are 3.125 Gbps, SMA connectors are used to ensure minimal loss. More information can be found about the DS25CP104 on the data sheets.

2. A **USB to SMBus converter** has been added to the evaluation kit to implement SMBus switch configuration to control the signal conditioning. Through the SMBus the DS25CP104 currently features four levels (Off, Low, Medium, and High) of pre-emphasis and two levels (Off, Low) of equalization.

3. **Three channels of stripline** have been added to the evaluation kit to test the pre-emphasis and equalization functions (15” (38.1cm), 30” (76.2cm), and 60” (152.4cm)). In practical applications, devices often drive long backplanes or cables. To help reduce jitter caused from long backplanes or cables, pre-emphasis can be used for the drivers and equalization for the receivers.

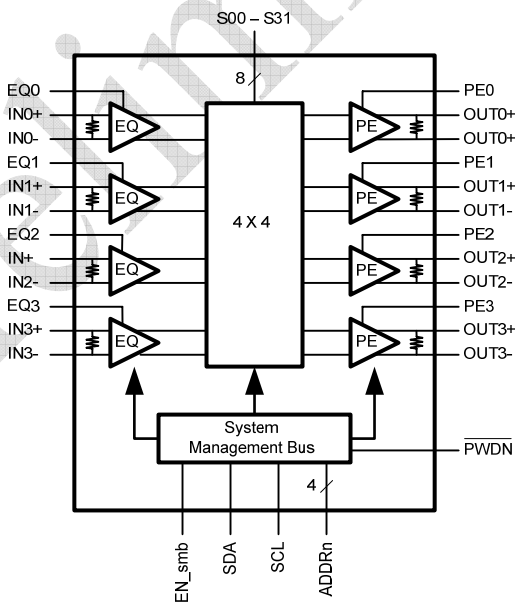


Figure 3. DS25CP104 Block Diagram

DS25CP104 Evaluation

The DS25CP104 is a 3.125 Gbps LVDS Crosspoint Switch with four levels of transmit pre-emphasis and two levels of receive equalization configured in the SMBus Mode and two levels of transmit pre-emphasis and two levels of receive equalization configured via external jumpers on the evaluation board in the Pin Mode.

Initial Pin Settings for Pin Mode Testing

Pin	Setting	Note
SMBus Enable	L	Disable SMbus
EQ0 – EQ 3	L	Equalization off, See table
PE0 – PE3	L	Pre-Emphasis off, See table
PWDN	H	Power Down off

Switch Configuration Truth Tables

S01	S00	Input Selected
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

Table 1. Input Select Pins Configuration for the Output OUT0

S11	S10	Input Selected
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

Table 2. Input Select Pins Configuration for the Output OUT1

S21	S20	Input Selected
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

Table 3. Input Select Pins Configuration for the Output OUT2

S31	S30	Input Selected
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

Table 4. Input Select Pins Configuration for the Output OUT3

Signal Conditioning Tables

Output OUTn, n={0,1,2,3}	
Pre-Emphasis Control Pin (PEn) State	**Pre-Emphasis Level**
0	Off
1	Medium

Table 5. Transmit Pre-emphasis Truth Table

Input INn, n={0,1,2,3}	
Equalization Control Pin (EQn) State	**Equalization Level**
0	Off
1	Low

Table 6. Receive Equalization Truth Table

Stripline Length Table (also known as Test Channels)

Stripline	Length	Loss (dB) @ 1250 MHz
L1	15” (38.1cm)	-3.6
L2	30” (76.2cm)	-8.2
L3	60” (152.4cm)	-14.5

Table 7. Stripline length table

Jitter Performance Testing with No Signal Conditioning

1. Configure the test setup as shown in Figure 4.

2. Set the desired INn to OUTn drivers by selecting S00, S01, S10, S11, S20, S21, S30, and S31 according to Tables 1 – 4.

3. Move the PEn and EQn jumpers to 0, according to tables 5 and 6.

4. Apply + supply (3.3V typical) to the VDD and – supply (ground) to the VSS connectors.

5. Connect a signal source (signal generator, data source, or an LVDS driver) to the desired INn inputs on the board and adjust the signal parameters (VOH, VOL, VCM) so that they comply with the device input recommendations. Either AC or DC coupling may be used on the inputs of the DS25CP104.

6. Connect an oscilloscope to the selected OUTn outputs and view the output signals with an oscilloscope with the bandwidth of at least 6 GHz. For most oscilloscopes, AC coupling of the outputs will be needed to properly load the LVDS outputs of the DS25CP104. Some newer differential probes, like the P7380SMA from Tektronix will automatically adjust to the LVDS output common mode voltage and no AC coupling is required.

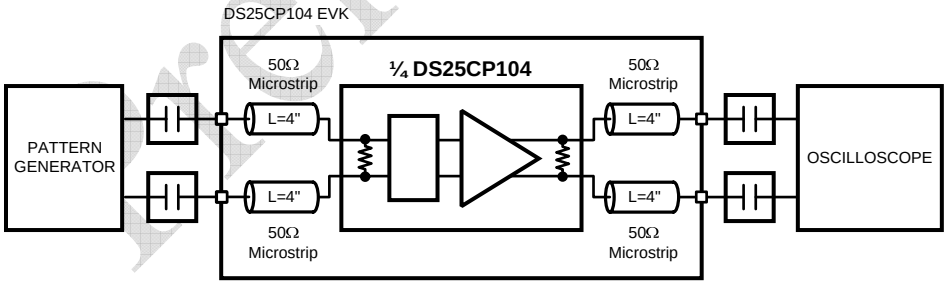


Figure 4. Jitter Performance Test Circuit

Pre-Emphasis Performance Testing

In applications where data transmits over cables or long backplanes, the pre-emphasis feature on the DS25CP104 transmitter helps to overcome media loss and reduce bit errors; hence the DS25CP104EVK has three lengths of stripline to test the pre-emphasis function.

1. Configure the test setup as shown in figure 5; select the desired test channel lengths in Table 7.

2. Set the desired INn to OUTn drivers by selecting S00, S01, S10, S11, S20, S21, S30 and S31 according to Tables 1 – 4.

3. Move the PEn jumpers to 1 and the EQn jumpers to 0, according to Tables 5 and 6.

4. Apply + supply (3.3V typical) to the VDD and – supply (ground) to the VSS connectors.

5. Connect a signal source (signal generator, data source, or an LVDS driver) to the desired INn inputs on the board and adjust the signal parameters (VOH, VOL, VCM) so that they comply with the device input recommendations. Either AC or DC coupling may be used on the inputs of the DS25CP104.

6. Connect an oscilloscope to the selected OUTn outputs and view the output signals with an oscilloscope with a bandwidth of at least 6 GHz. For most oscilloscopes, AC coupling of the outputs will be needed to properly load the LVDS outputs of the DS25CP104. Some newer differential probes, like the P7380SMA from Tektronix will automatically adjust to the LVDS output common mode voltage and no AC coupling is required.

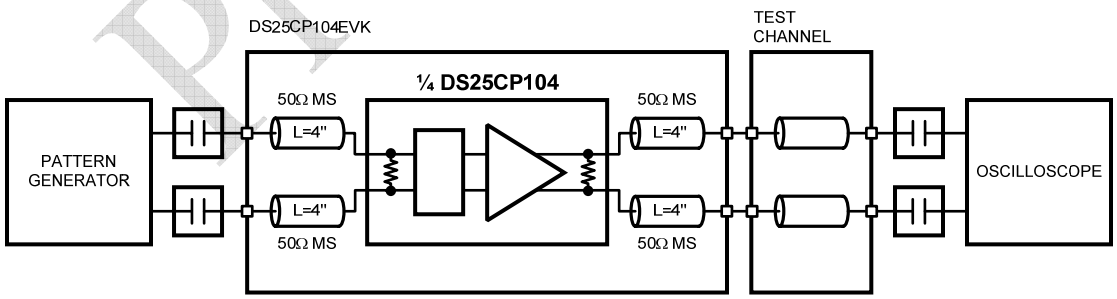


Figure 5. Pre-Emphasis Performance Test Circuit

Equalization Performance Testing

In some applications, data transmits over cables or long backplanes. The equalization function on the DS25CP104 receivers helps to compensate for loss of certain media; hence the DS25CP104EVK has three lengths of stripline to test the equalization function.

1. Configure the test setup as shown in Figure 6; select the desired test channel, lengths in Table 7.

2. Set the desired INn to OUTn drivers by selecting S00, S01, S10, S11, S20, S21, S30, S31 according to Tables 1 – 4.

3. Select the PEn jumpers to 0 and the EQn jumpers to 1, according to Tables 5 and 6.

4. Apply + supply (3.3V typical) to the VDD and – supply (ground) to the VSS connectors.

5. Connect a signal source (signal generator, data source, or an LVDS driver) to the desired INn inputs on the board and adjust the signal parameters (VOH, VOL, VCM) so that they comply with the device input recommendations. Either AC or DC coupling may be used on the inputs of the DS25CP104.

6. Connect an oscilloscope to the selected OUTn outputs and view the output signals with an oscilloscope with a bandwidth of at least 6 GHz. For most oscilloscopes, AC coupling of the outputs will be needed to properly load the LVDS outputs of the DS25CP104. Some newer differential probes, like the P7380SMA from Tektronix will automatically adjust to the LVDS output common mode voltage and no AC coupling is required.

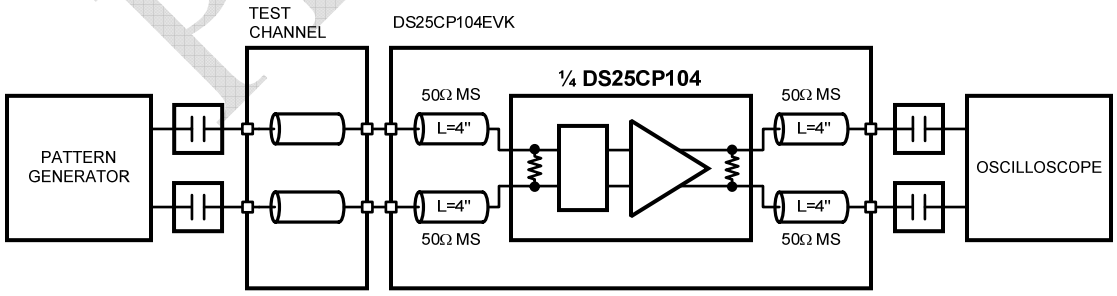


Figure 6. Equalization Performance Test Circuit

Pre-Emphasis and Equalization Performance Testing

In some applications, data transmits over cables or long backplanes. The pre-emphasis and equalization functions on the DS25CP104 help to compensate for loss of certain media; hence the DS25CP104EVK has three lengths of stripline to test the pre-emphasis and equalization functions.

1. Configure the test setup as shown in Figure 7; select the desired test channel, lengths in Table 7.

2. Set the desired INn to OUTn drivers by selecting S00, S01, S10, S11, S20, S21, S30, and S31 according to Tables 1 – 4.

3. Select the PEn jumpers to 1 and the EQn jumpers to 1, according to Tables 5 and 6.

4. Apply + supply (3.3V typical) to the VDD and – supply (ground) to the VSS connectors.

5. Connect a signal source (signal generator, data source, or an LVDS driver) to the desired INn inputs on the board and adjust the signal parameters (VOH, VOL, VCM) so that they comply with the device input recommendations. Either AC or DC coupling may be used on the inputs of the DS25CP104.

6. Connect an oscilloscope to the selected OUTn outputs and view the output signals with an oscilloscope with a bandwidth of at least 6 GHz. For most oscilloscopes, AC coupling of the outputs will be needed to properly load the LVDS outputs of the DS25CP104. Some newer differential probes, like the P7380SMA from Tektronix will automatically adjust to the LVDS output common mode voltage and no AC coupling is required.

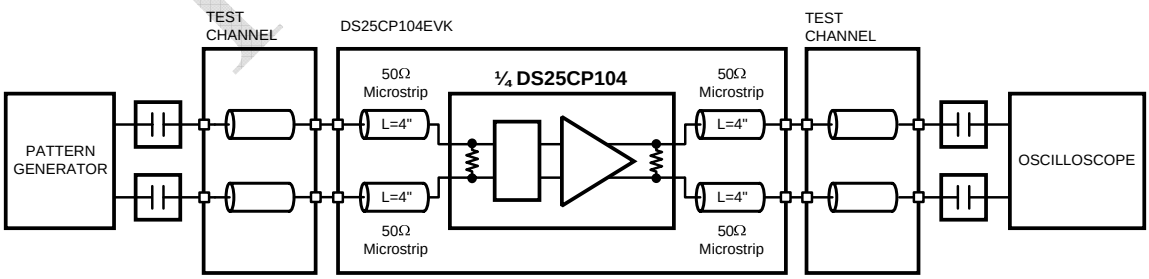


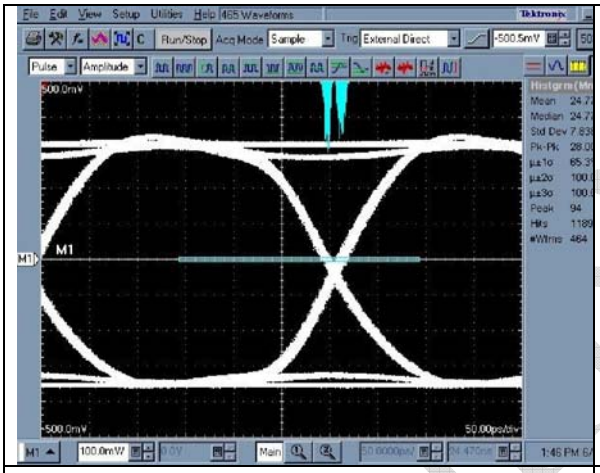
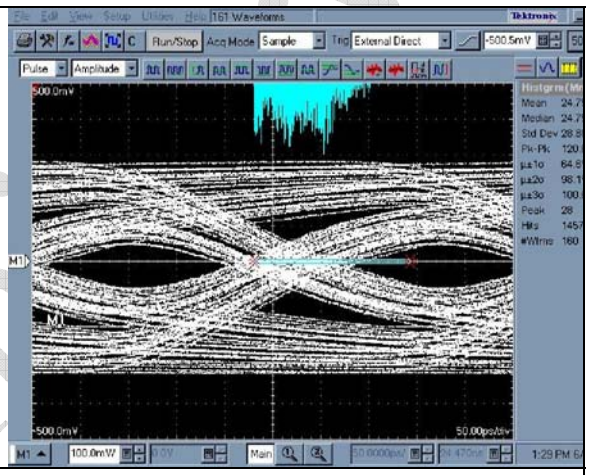
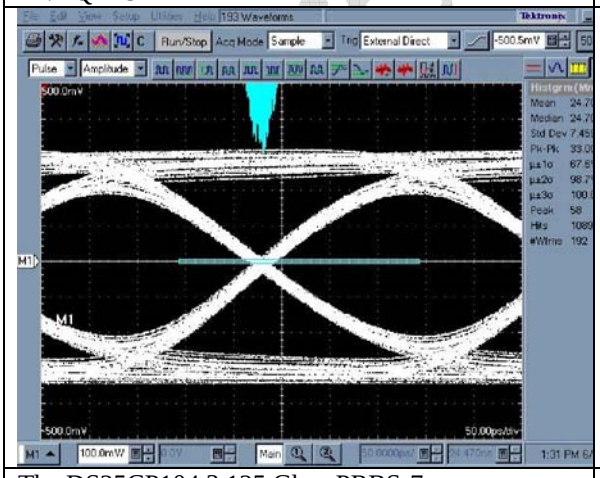
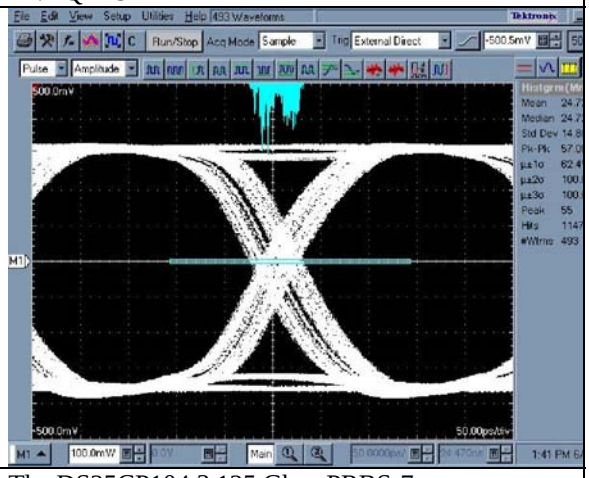
Figure 7. Pre-emphasis and Equalization Performance Test Circuit

SMBus Evaluation

The description of the USB to SMBus function of the DS25CP104EVK will follow in future revisions of this user manual. The full range of crosspoint switch configurations are possible using the configuration control pin jumpers.

Typical Performance

This section of the User Manual shows typical eye diagrams you can expect to see when evaluating the DS25CP104EVK.

	
The DS25CP104 3.125 Gbps PRBS-7 output eye diagram with no STRIPLINE connected and with PE/EQ = Off	The DS25CP104 3.125 Gbps PRBS-7 output eye diagram after the STRIPLINE2 (30” FR4) and with PE/EQ = Off
	
The DS25CP104 3.125 Gbps PRBS-7 output eye diagram after the STRIPLINE 2 (30” FR4) and with PE = Med. See Figure 5 for the Setup used.	The DS25CP104 3.125 Gbps PRBS-7 output eye diagram after the STRIPLINE 1 (15” FR4) and with EQ = Low. See Figure 6 for the Setup used.

ENERCON - BILL OF MATERIALS	TITLE: NATIONAL SEMICONDUCTOR PCBA, DS25CP104EVK, ROHS	PL Number: Z3071-01	Rev: 0	Rev By:	Rev Date: 3/28/2007	PL Status: Released
Main Product: PCBA, DS25CP104 EVK		Responsible Eng/Mgr:		Creator: Arlene Fox		Creation Date: 3/28/2007

Item	Part Type	Part Number/Value	Mfg	NoSub	Description	Qty	SMT	Ref Des	Notes	Rev
1	PCB	P-05885R0			DS25CP104EVK: 5.25x5.25x.060in, 8 layer	1			Bd: (133.35x 133.35mm) Panel: (10.60x5.25in) (269.24x 133.35mm) 2 bds/panel	0
2										
3	IC	24LC128-I/SN	MICROCHIP		128K bit Serial EEPROM 2.5V, SOIC8, Pb-Free	1	X	U3		0
4	IC	CY7C68013A-56LFXC	CYPRESS		EZ-USB FX2 USB Microcontroller, QFN56, Pb-Free	1	X	U1		0
5	IC	DS25CP104	NAT			1		U5	Customer Supplied	0
6	IC	LP38691SD-3.3/NOPB	NAT		Linear Regulator, 3.3V, LLP6, Pb-Free	1	X	U2		0
7	IC	PGB1040805	LF		ESD Suppressor, 0805, Pb-Free	1	X	U4		0
8										
9	RES	ERJ-3GEY0R00	PANA		0 Ohm 1/10W ±5% 0603, Pb-Free	3	X	R4,5,14		0
	<ALT>	CRCW06030000Z0EA	VISHAY		0 Ohm 1/10W ±5% 0603, Pb-Free					
	<ALT>	MCR03EZPJ000	ROHM		0 Ohm 1/10W ±5% 0603, Pb-Free					
	<ALT>	RC0603JR-070RL	YAGEO		0 Ohm 1/10W ±5% 0603, Pb-Free					
10	RES	ERJ-3GEYJ103	PANA		10K 1/10W ±5% 0603 200ppm, Pb-Free	5	X	R3,8-9,12,13		0
	<ALT>	CRCW060310K0JNEA	VISHAY		10K 1/10W ±5% 0603 200ppm, Pb-Free					
	<ALT>	RK73B1JTTD103J	KOA		10K 1/10W ±5% 0603 200ppm, Pb-Free					
11	RES	ERJ-3GEYJ220	PANA		22 Ohm 1/10W ±5% 0603 200ppm, Pb-Free	2	X	R1-2		0
	<ALT>	CRCW060322R0JNEA	VISHAY		22 Ohm 1/10W ±5% 0603 200ppm, Pb-Free					
	<ALT>	RK73B1JTTD220J	KOA		22 Ohm 1/10W ±5% 0603 200ppm, Pb-Free					
12	RES	ERJ-3GEYJ222	PANA		2.2K 1/10W ±5% 0603 200ppm, Pb-Free	2	X	R6,7		0
	<ALT>	CRCW06032K20JNEA	VISHAY		2.2K 1/10W ±5% 0603 200ppm, Pb-Free					
	<ALT>	RK73B1JTTD222J	KOA		2.2K 1/10W ±5% 0603 200ppm, Pb-Free					
13	RES	ERJ-8GEY0R00	PANA		0 Ohm 1/4W ±5% 1206, Pb-Free	2	X	R10-11		0

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Main Product: PCBA, DS25CP104 EVK		Responsible Eng/Mgr:		Creator: Arlene Fox	Creation Date: 3/28/2007	

Item	Part Type	Part Number/Value	Mfg	NoSub	Description	Qty	SMT	Ref Des	Notes	Rev
	<ALT>	CRCW12060000Z0EA	VISHAY		0 Ohm 1/4W ±5% 1206, Pb-Free					
14										
15	CAP	0402YC103KAT	AVX		.01µF, 16V, ±10%, 0402, Ceramic, X7R, Pb-Free	2	X	C15,17		0
	<ALT>	C0402C103K4RAC	KEMET		.01µF, 16V, ±10%, 0402, Ceramic, X7R, Pb-Free					
	<ALT>	ECJ-0EB1C103K	PANA		.01µF, 16V, ±10%, 0402, Ceramic, X7R, Pb-Free					
16	CAP	08055A180JAT	AVX		18pF, 50V, ±5%, 0805, Ceramic, NP0, Pb-Free	2	X	C11-12		0
	<ALT>	C0805C180J5GAC	KEMET		18pF, 50V, ±5%, 0805, Ceramic, NP0, Pb-Free					
	<ALT>	ECJ-2VC1H180J	PANA		18pF, 50V, ±5%, 0805, Ceramic, NP0, Pb-Free					
17	CAP	C0402C104K8RAC	KEMET		.1µF, 10V, ±10%, 0402, Ceramic, X7R, Pb-Free	10	X	C1,4-8,10,13-14,16		0
18	CAP	C1206C225K4RAC	KEMET		2.2µF, 16V, ±10%, 1206, Ceramic, X7R, Pb-Free	4	X	C2,3,9,18		0
	<ALT>	ECJ-3YB1C225K	PANA		2.2µF, 16V, ±10%, 1206, Ceramic, X7R, Pb-Free					
19										
20	FILTER	MMZ1608R301A	TDK		Ferrite, 300 Ohm, .5A, 0603, Pb Free	2	X	FB1-2		0
21										
22	XTAL	HCM49-24.000MABJ	CITIZEN		Crystal, 24.0000MHz, SMD, 18pF, Pb-Free	1	X	Y1		0
23										
24	FUSE	1206L050	LF		.5A, Resettable, SMT, .09 Ohms, Pb Free	1	X	F1		0
25										
26	CONN	1287-ST	KEYSTONE		Faston, Male, .250x.032, Pb-Free	2		J25-26		0
27	CONN	142-0701-851	EMERSON		SMA, Jack Receptacle, 50 OHM, Pb-Free	28		SMA1-28		0
28	CONN	61729-0010	FCI		USB-B, 4p, R/A, Pb-Free	1		J1		0
29	CONN	TSW-102-07-G-S	SAMTEC		Header, 2p, Male, .100"sp, Gold, Pb-Free	2		J3-4		0
30	CONN	TSW-103-07-G-S	SAMTEC		Header, 3p, Male, .100"sp, Gold, Pb-Free	18		J7-24		0

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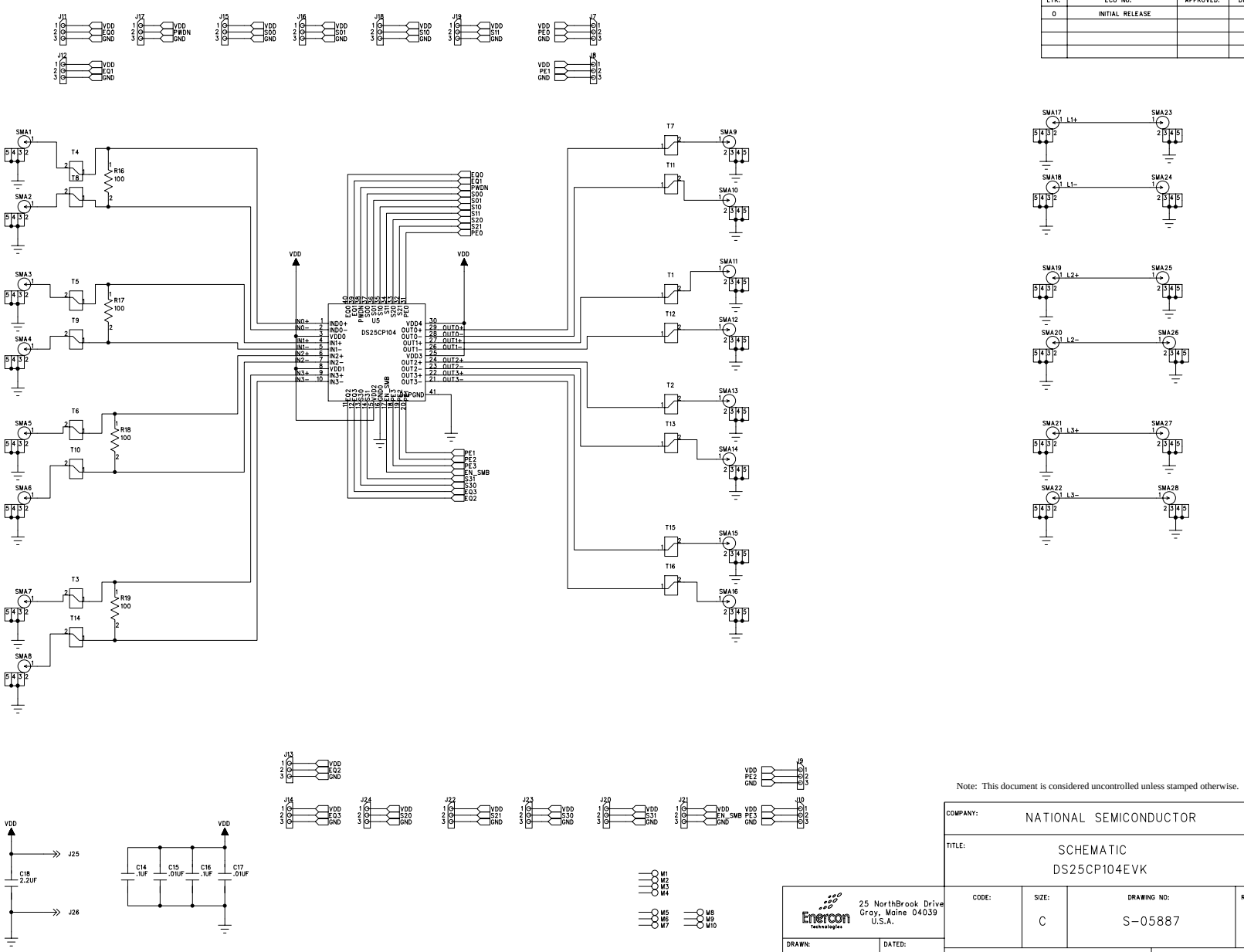
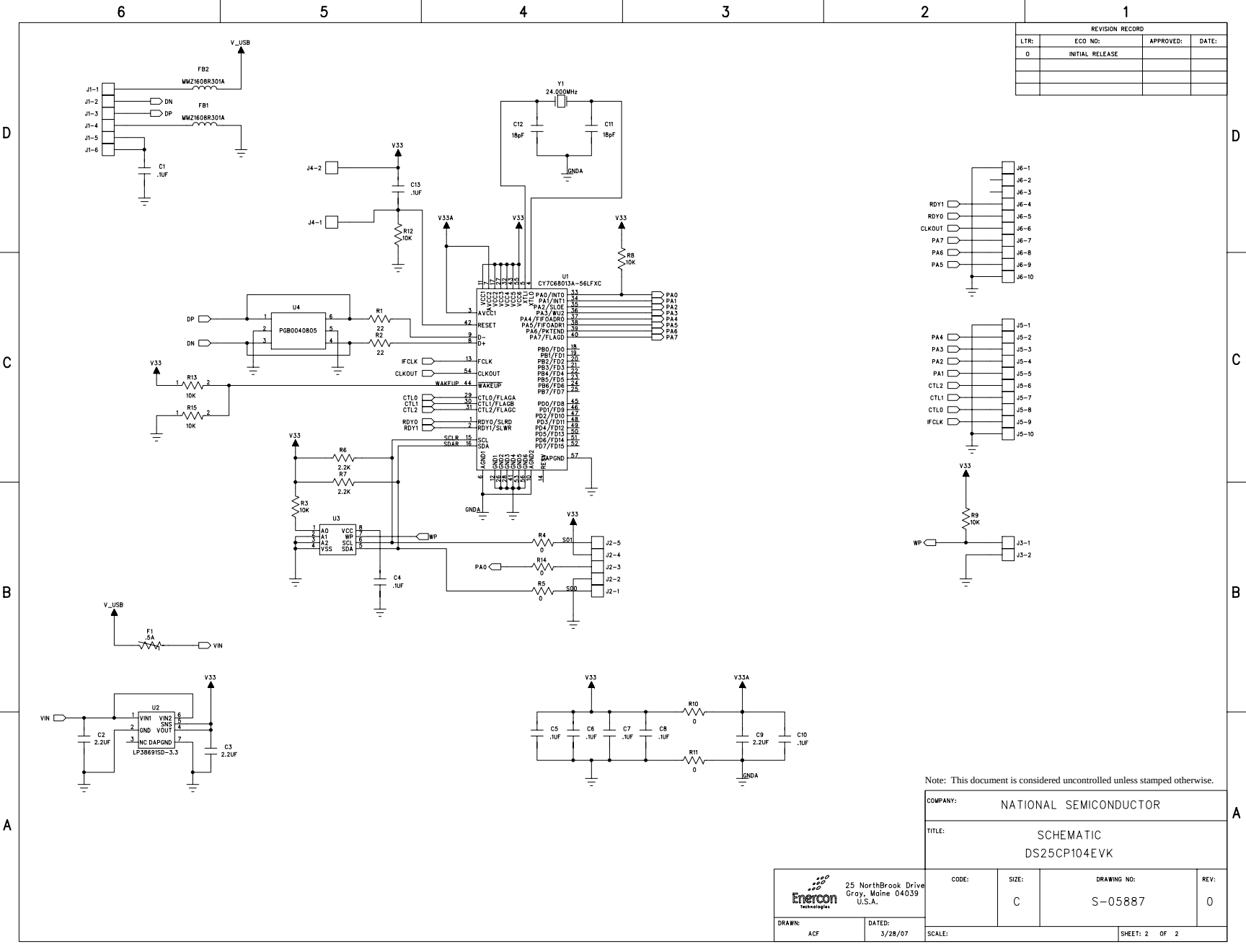
Item	Part Type	Part Number/Value	Mfg	NoSub	Description	Qty	SMT	Ref Des	Notes	Rev
31	CONN	TSW-105-07-G-S	SAMTEC		Header, 5p, Male, .100"sp, Gold, Pb-Free	1		J2		0
32										
33	STENCL	T-05889R0	ENERCON		STENCIL FABRICATION, TOP, DS25CP104EVK	1				0
34	STENCL	T-05890R0	ENERCON		STENCIL FABRICATION, BOTTOM, DS25CP104EVK	1				0
35										
36	REF	C-05886R0	ENERCON		FABRICATION DWG, DS25CP104EVK					0
37	REF	C-05888R0	ENERCON		PALLET DWG, DS25CP104EVK					0
38	REF	S-05887R0	ENERCON		SCHEMATIC, DS25CP104EVK					0
39										
40										
41										

Notes:

DO NOT STUFF:

R15,16,17,18,19
J5,6


REVISION RECORD
LTR: | ECO NO: | APPROVED: | DATE:
0 | INITIAL RELEASE
DS25CP104
U5
SMA1
SMA2
SMA3
SMA4
SMA5
SMA6
SMA7
SMA8
SMA9
SMA10
SMA11
SMA12
SMA13
SMA14
SMA15
SMA16
SMA17
SMA18
SMA19
SMA20
SMA21
SMA22
SMA23
SMA24
SMA25
SMA26
SMA27
SMA28
R16 100
R17 100
R18 100
R19 100
C14 .1UF
C15 .01UF
C16 .1UF
C17 .01UF
C18 2.2UF
VDD
GND
Note: This document is considered uncontrolled unless stamped otherwise.
COMPANY: NATIONAL SEMICONDUCTOR
TITLE: SCHEMATIC DS25CP104EVK
Enercon Technologies
25 NorthBrook Drive
Gray, Maine 04039
U.S.A.
CODE:
SIZE: C
DRAWING NO: S-05887
REV: 0
DRAWN: ACF
DATED: 3/28/07
SCALE:
SHEET: 1 OF 2


REVISION RECORD
LTR: ECO NO: APPROVED: DATE:
0 INITIAL RELEASE
V_USB
FB2
MMZ1608R301A
FB1
MMZ1608R301A
J1-1
J1-2
J1-3
J1-4
J1-5
J1-6
DN
DP
C1
.1UF
Y1
24.000MHz
C12
18pF
C11
18pF
GNDA
V33
J4-2
J4-1
C13
.1UF
R12
10K
V33A
R8
10K
U1
CY7C68013A-56LFXC
PA0/INT0
PA1/INT1
PA2/SLOE
PA3/WU2
PA4/FIFOADR0
PA5/FIFOADR1
PA6/PKTEND
PA7/FLAGD
PB0/FD0
PB1/FD1
PB2/FD2
PB3/FD3
PB4/FD4
PB5/FD5
PB6/FD6
PB7/FD7
PD0/FD8
PD1/FD9
PD2/FD10
PD3/FD11
PD4/FD12
PD5/FD13
PD6/FD14
PD7/FD15
AVCC1
RESET
D-
D+
FCLK
CLKOUT
WAKEUP
CTL0/FLAGA
CTL1/FLAGB
CTL2/FLAGC
RDY0/SLRD
RDY1/SLWR
SCL
SDA
AGND
GND
RSVD
EXTAGND
U4
PGB0040805
R1
22
R2
22
R13
10K
R15
10K
R6
2.2K
R7
2.2K
R3
10K
U3
A0
A1
A2
VSS
VCC
WP
SCL
SDA
C4
.1UF
R4
0
R14
0
R5
0
S01
S00
J2-5
J2-4
J2-3
J2-2
J2-1
PA0
WP
J6-1
J6-2
J6-3
J6-4
J6-5
J6-6
J6-7
J6-8
J6-9
J6-10
RDY1
RDY0
CLKOUT
PA7
PA6
PA5
J5-1
J5-2
J5-3
J5-4
J5-5
J5-6
J5-7
J5-8
J5-9
J5-10
PA4
PA3
PA2
PA1
CTL2
CTL1
CTL0
IFCLK
R9
10K
J3-1
J3-2
V_USB
F1
.5A
VIN
U2
VIN1
VIN2
SNS
GND
VOUT
NC DAPGND
LP38691SD-3.3
C2
2.2UF
C3
2.2UF
C5
.1UF
C6
.1UF
C7
.1UF
C8
.1UF
R10
0
R11
0
C9
2.2UF
C10
.1UF
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COMPANY: NATIONAL SEMICONDUCTOR
TITLE: SCHEMATIC
DS25CP104EVK
Enercon Technologies
25 NorthBrook Drive
Gray, Maine 04039
U.S.A.
CODE:
SIZE: C
DRAWING NO: S-05887
REV: 0
DRAWN: ACF
DATED: 3/28/07
SCALE:
SHEET: 2 OF 2

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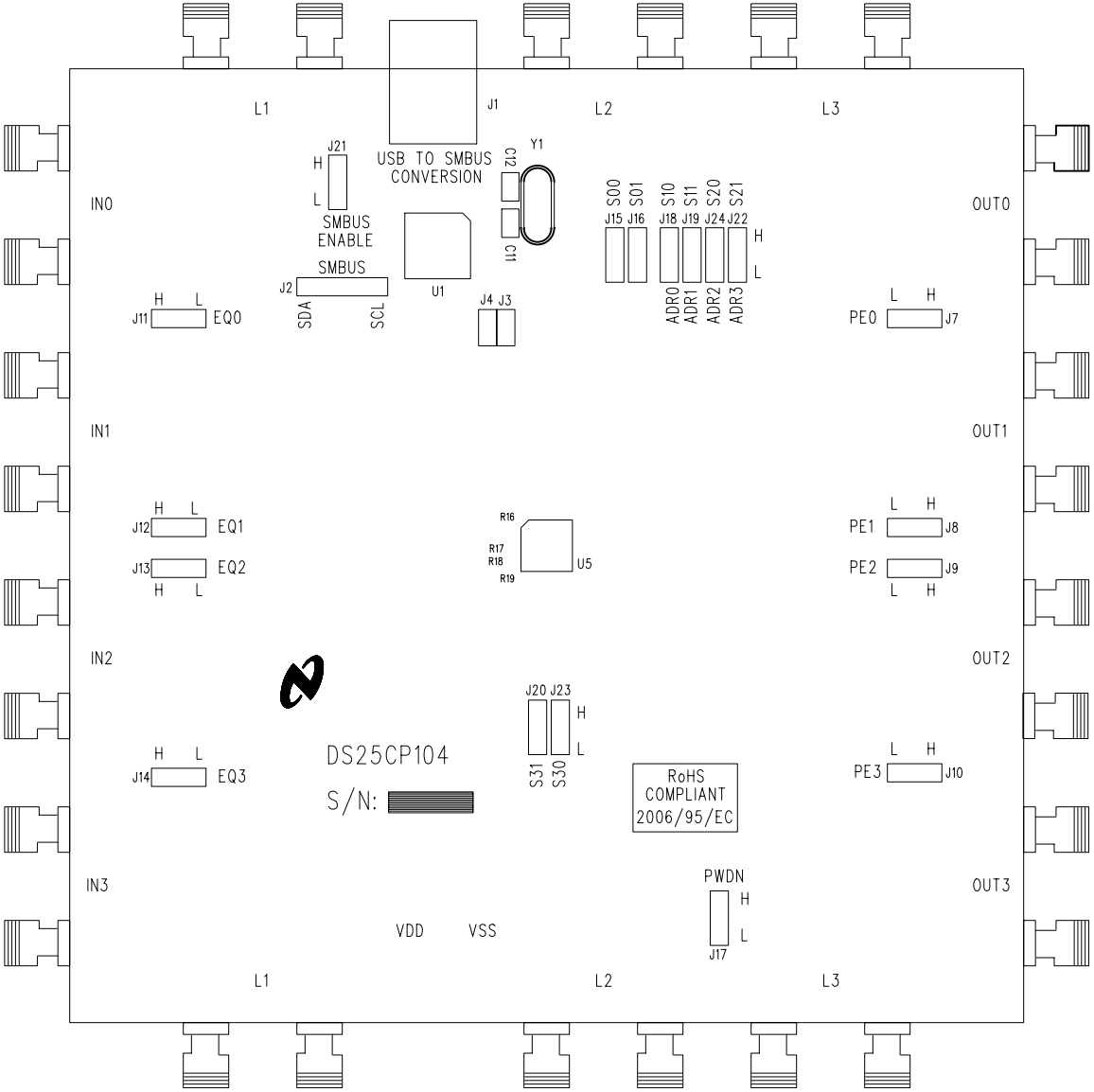

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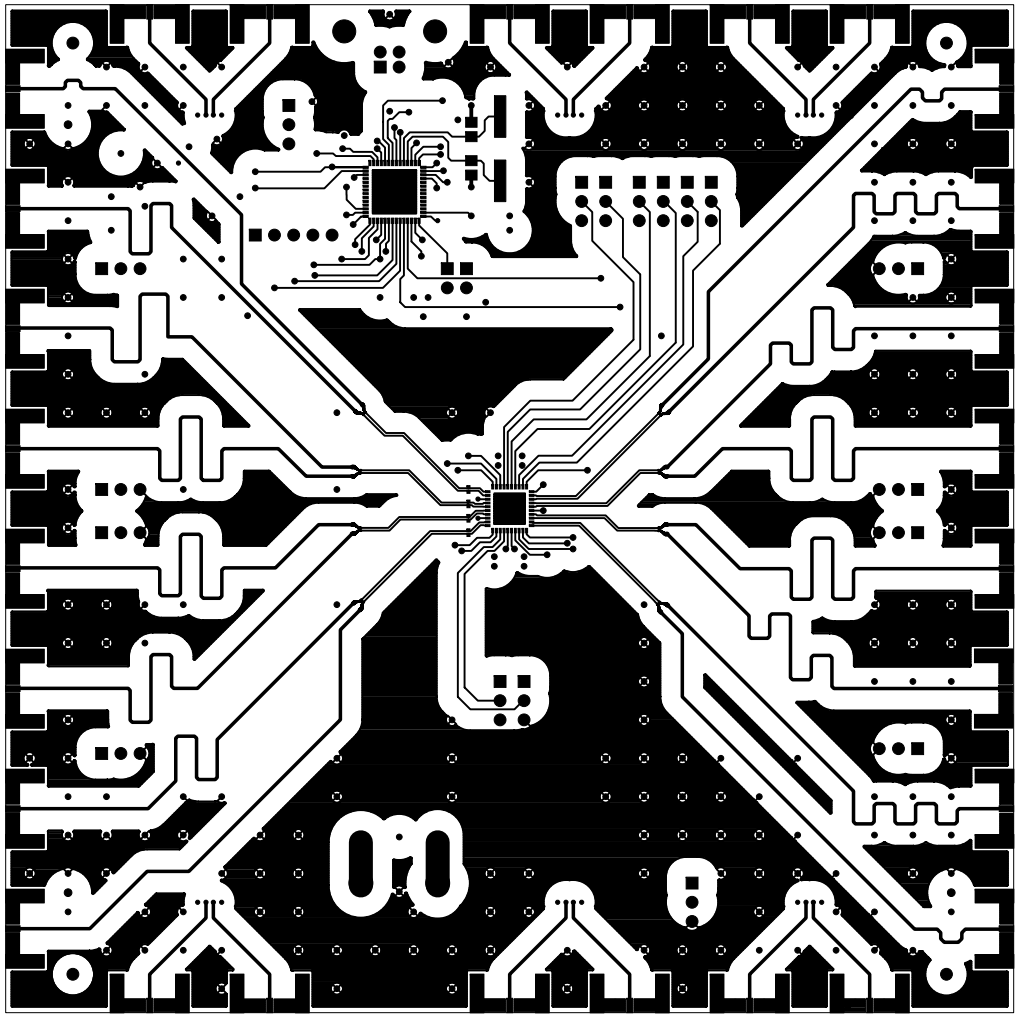

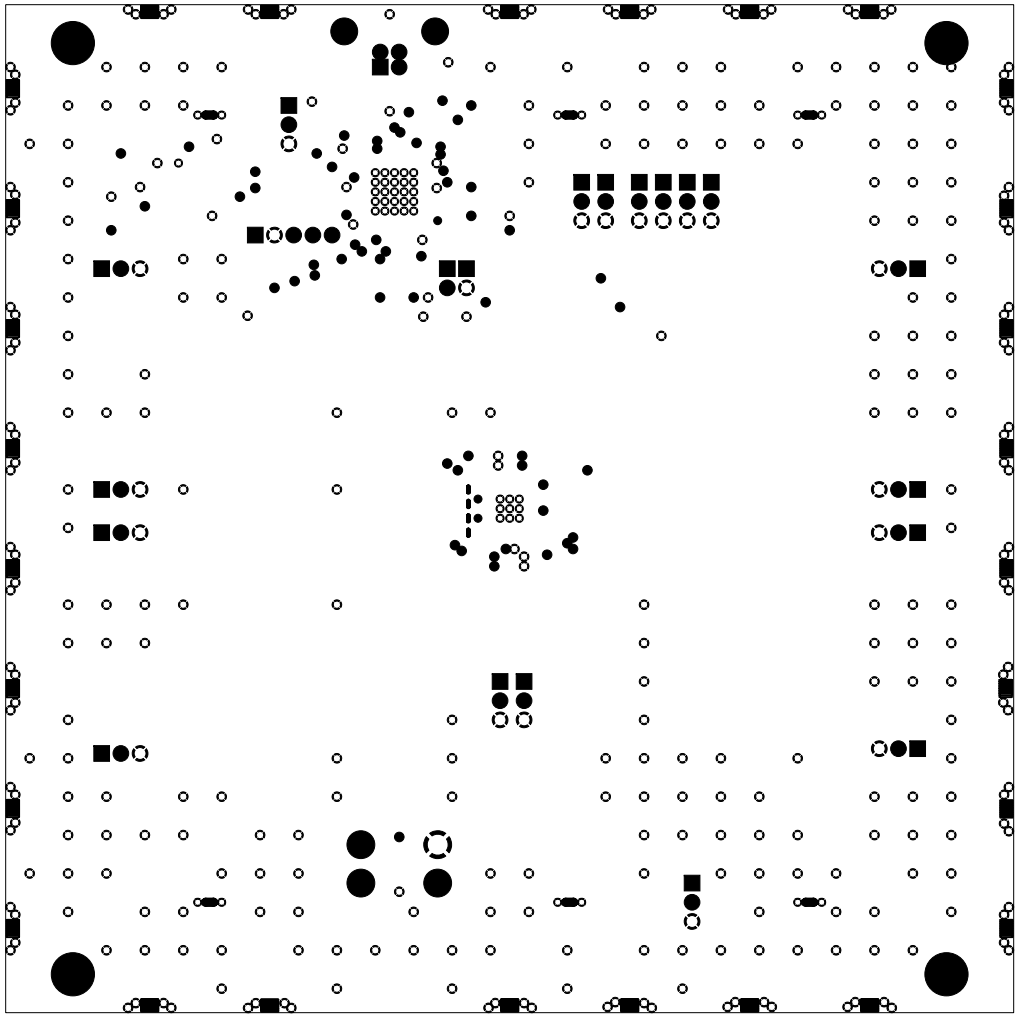

LAYER 2 GND PLANE

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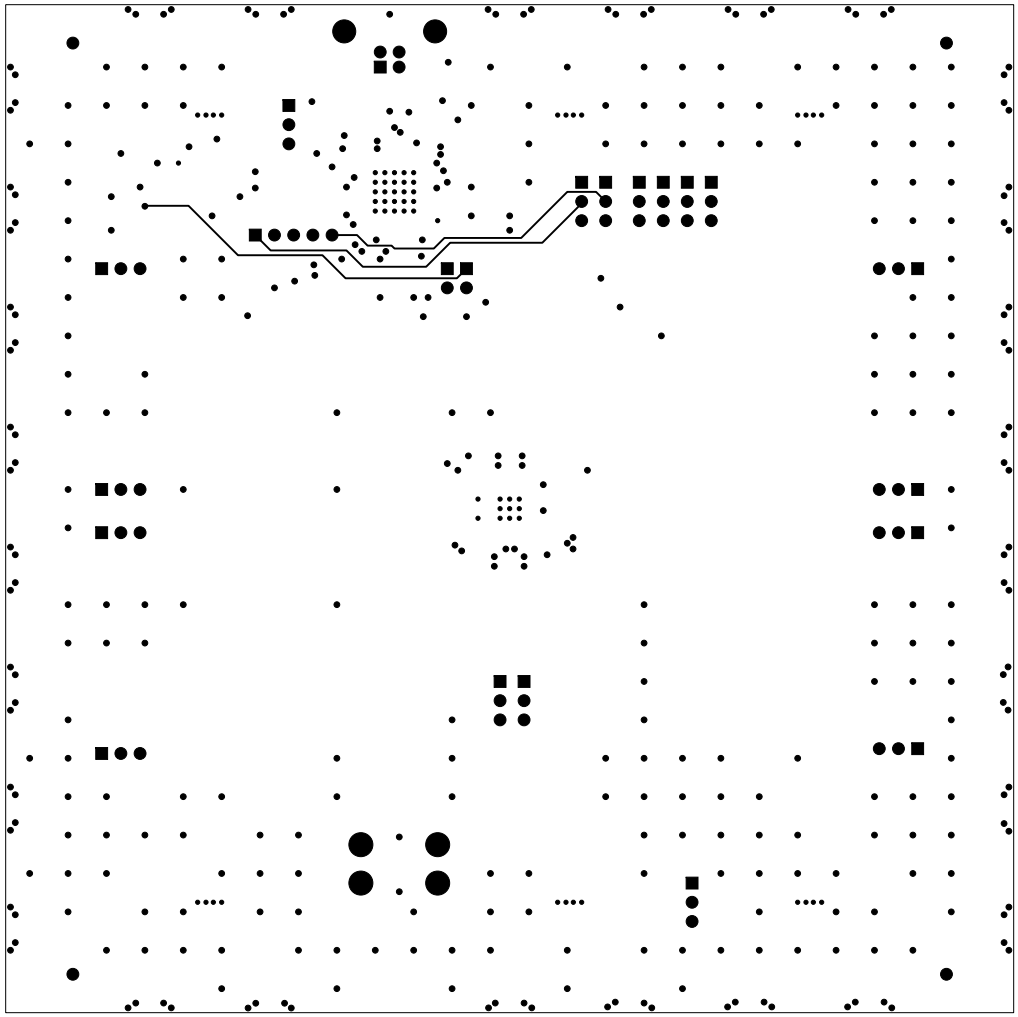

LAYER 3 SIGNAL

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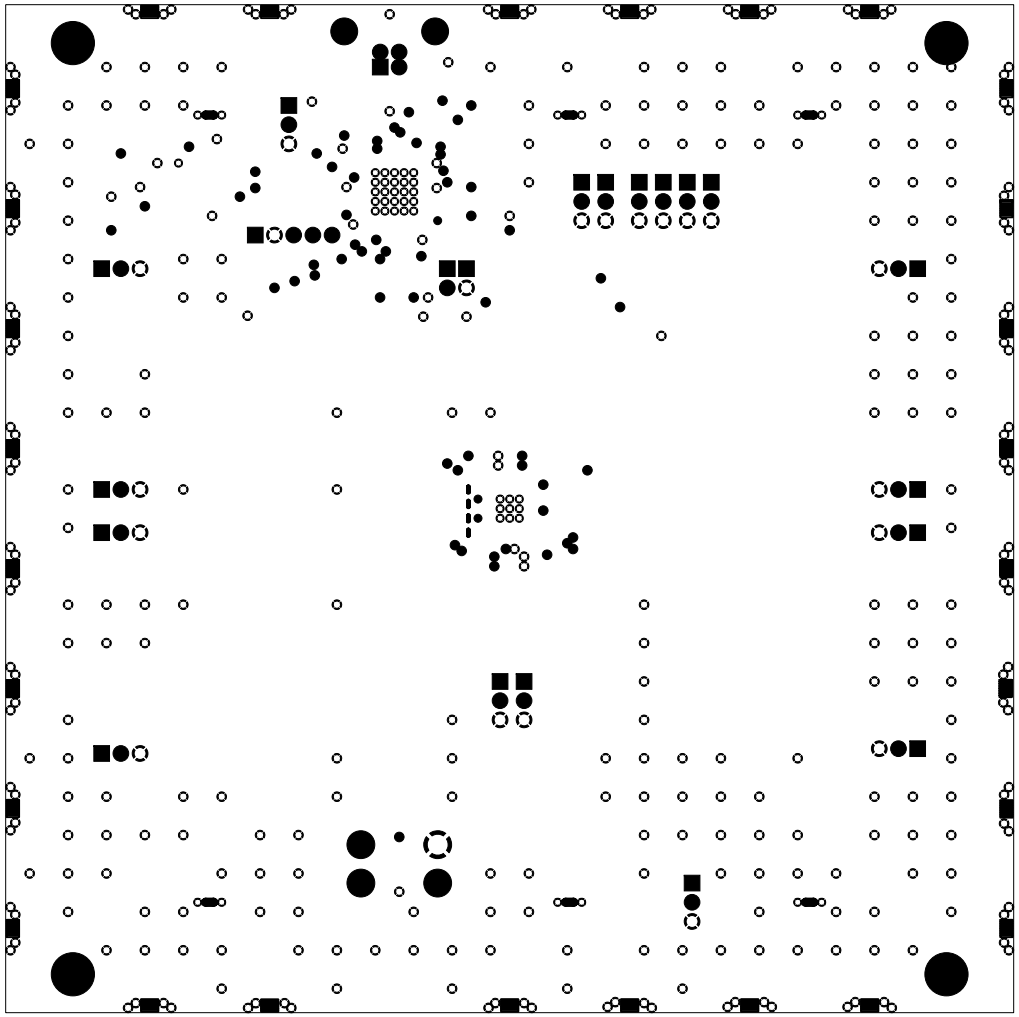
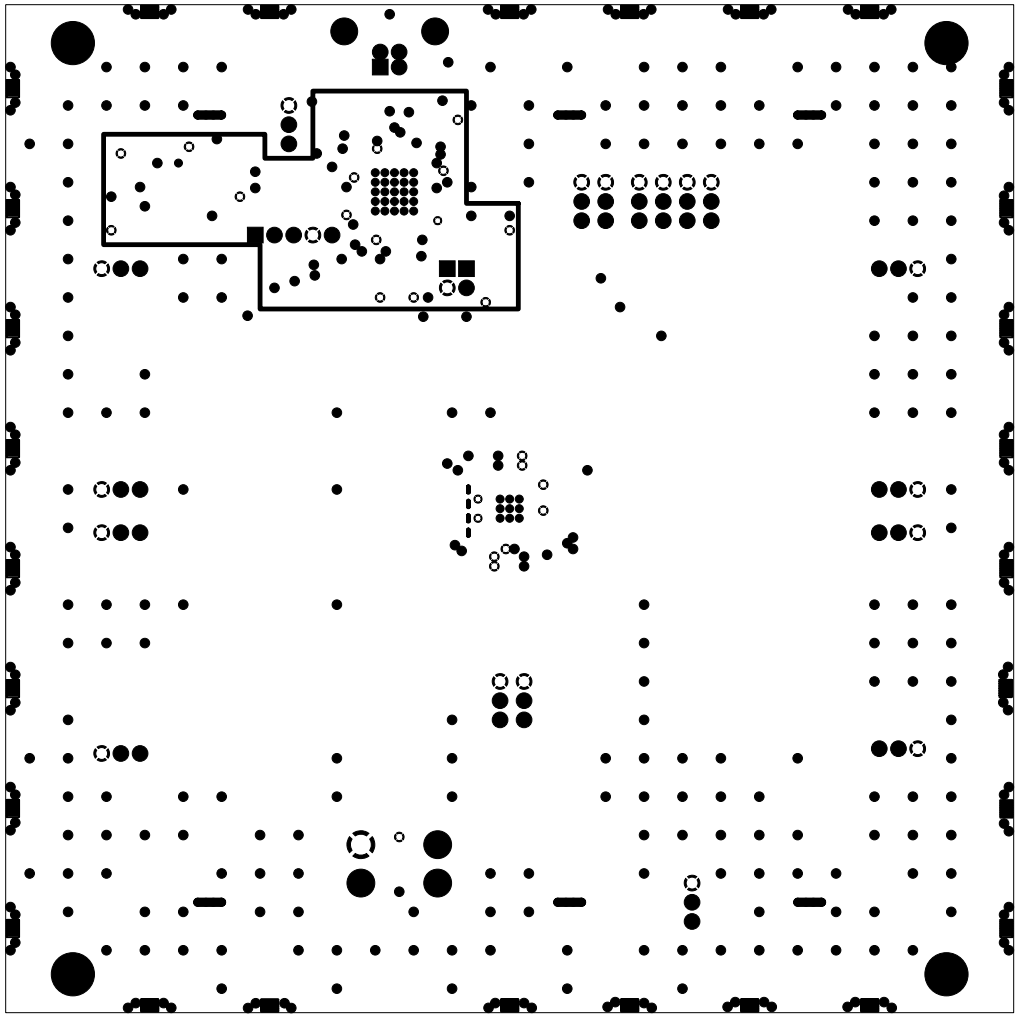


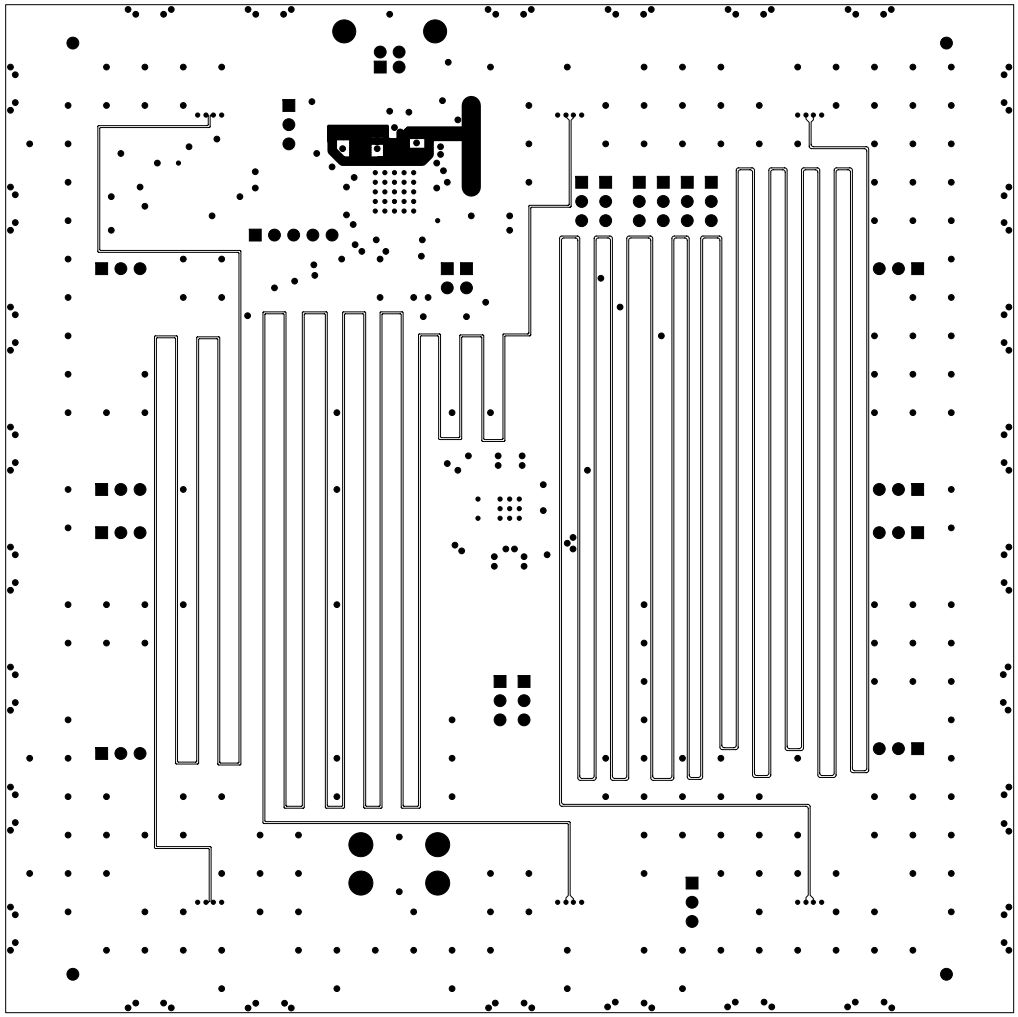
LAYER 4 GND PLANE

Note: This document is considered uncontrolled unless stamped otherwise.



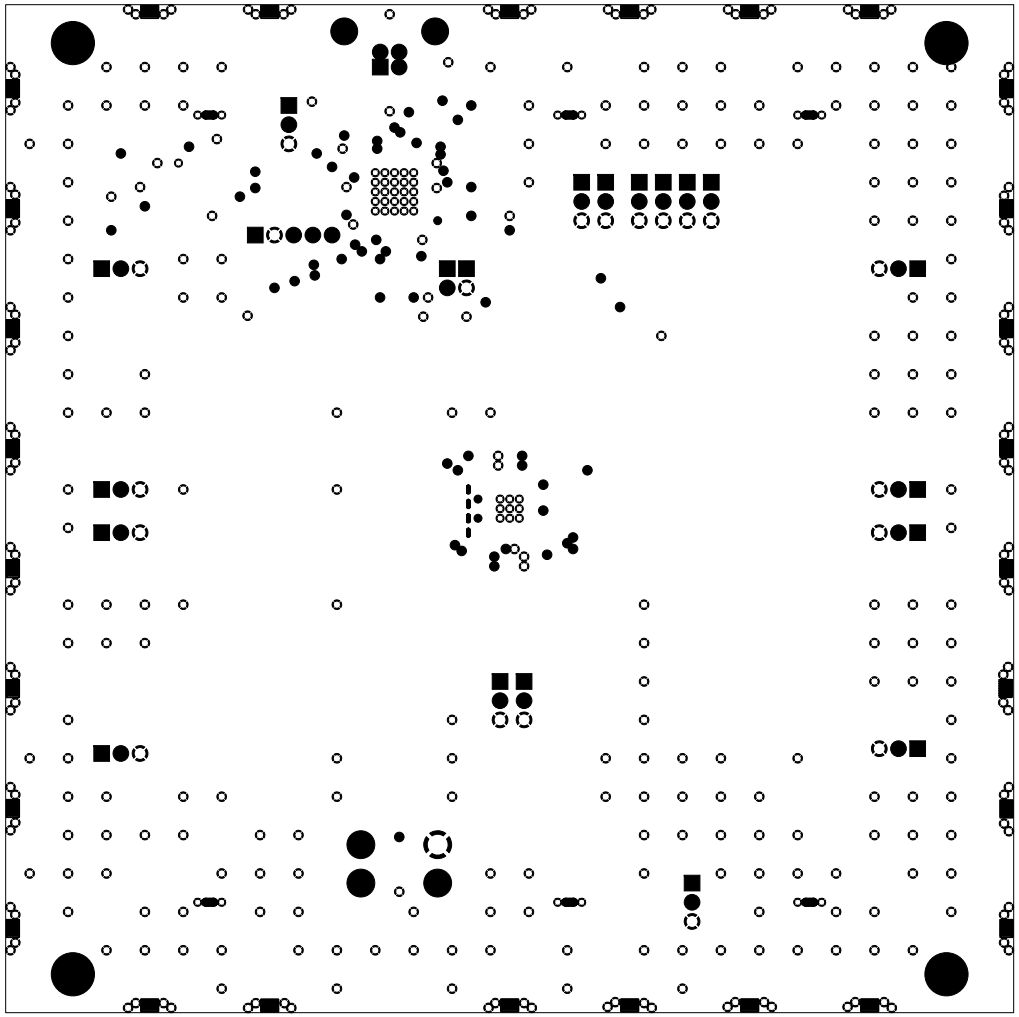
LAYER 5 VCC PLANE

Note: This document is considered uncontrolled unless stamped otherwise.



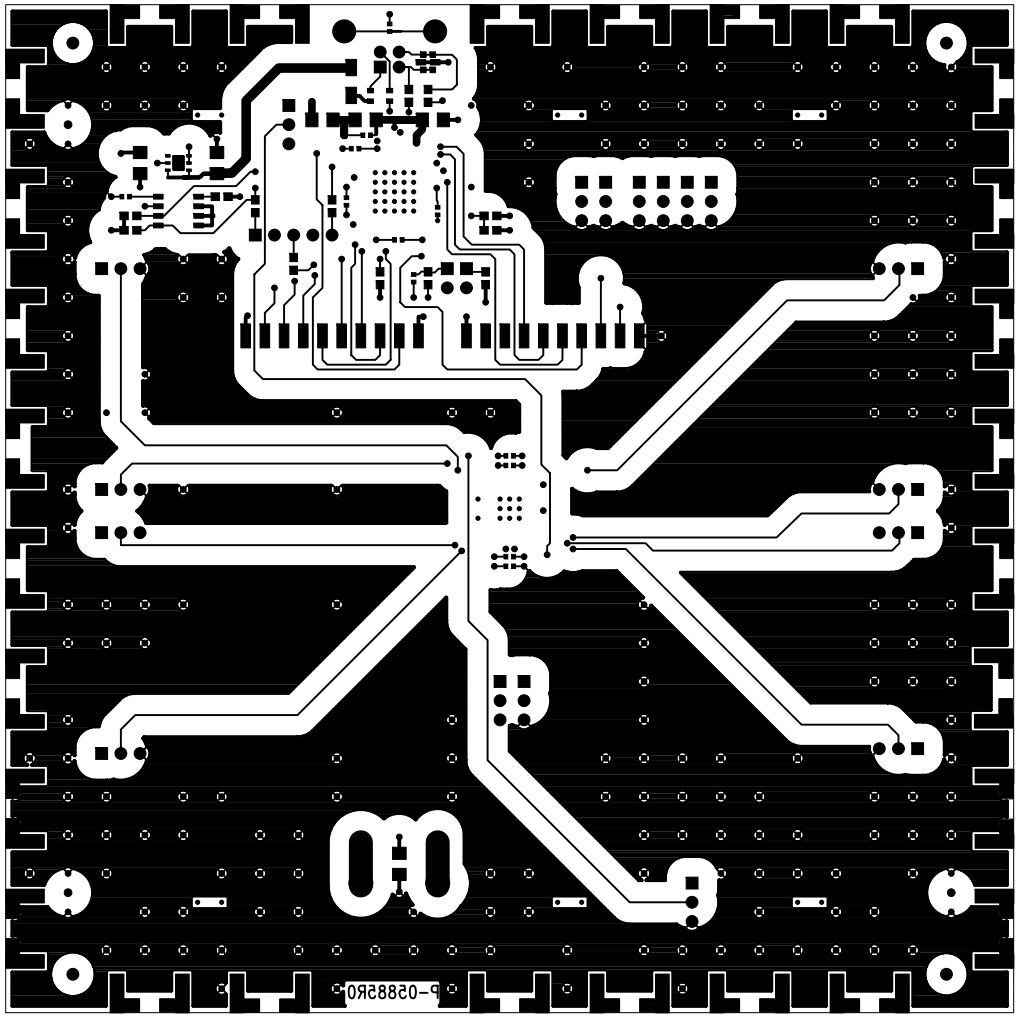
LAYER 6 SIGNAL

Note: This document is considered uncontrolled unless stamped otherwise.

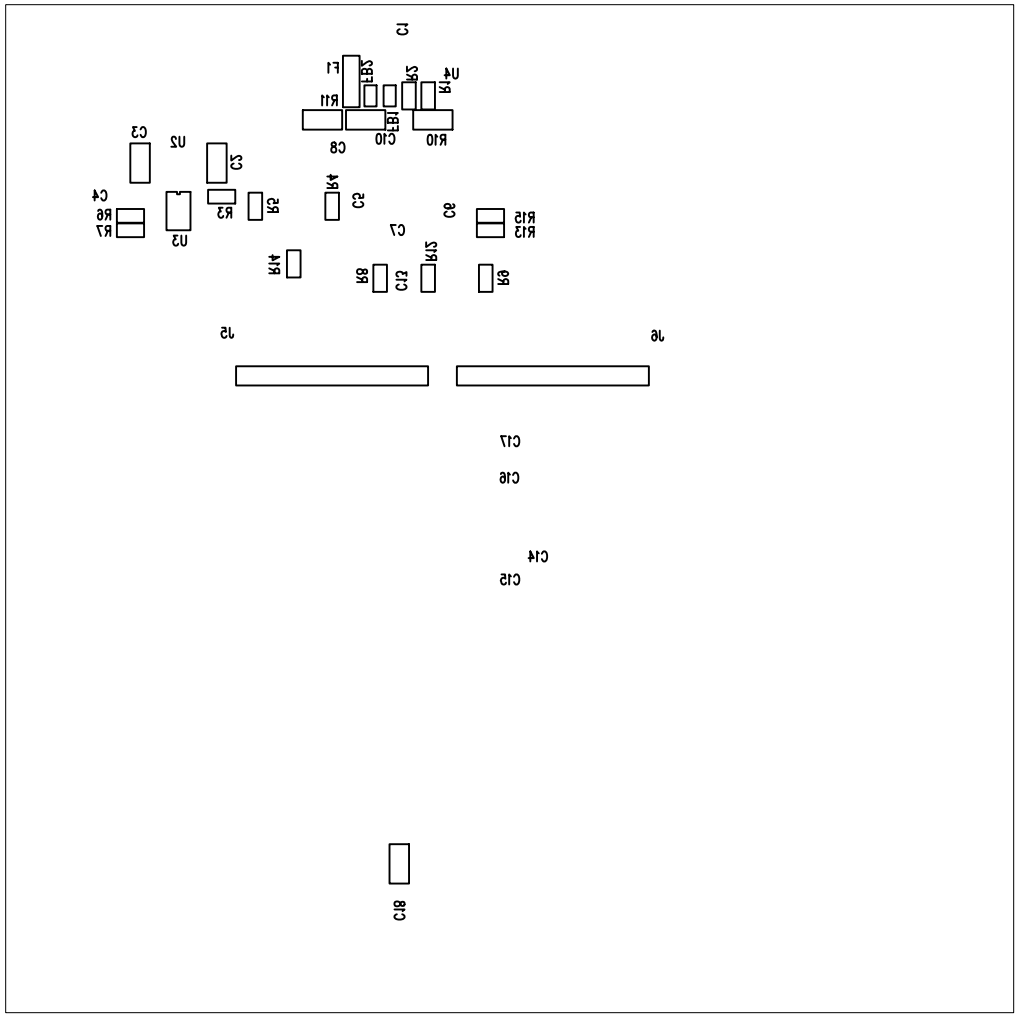


LAYER 7 GND PLANE

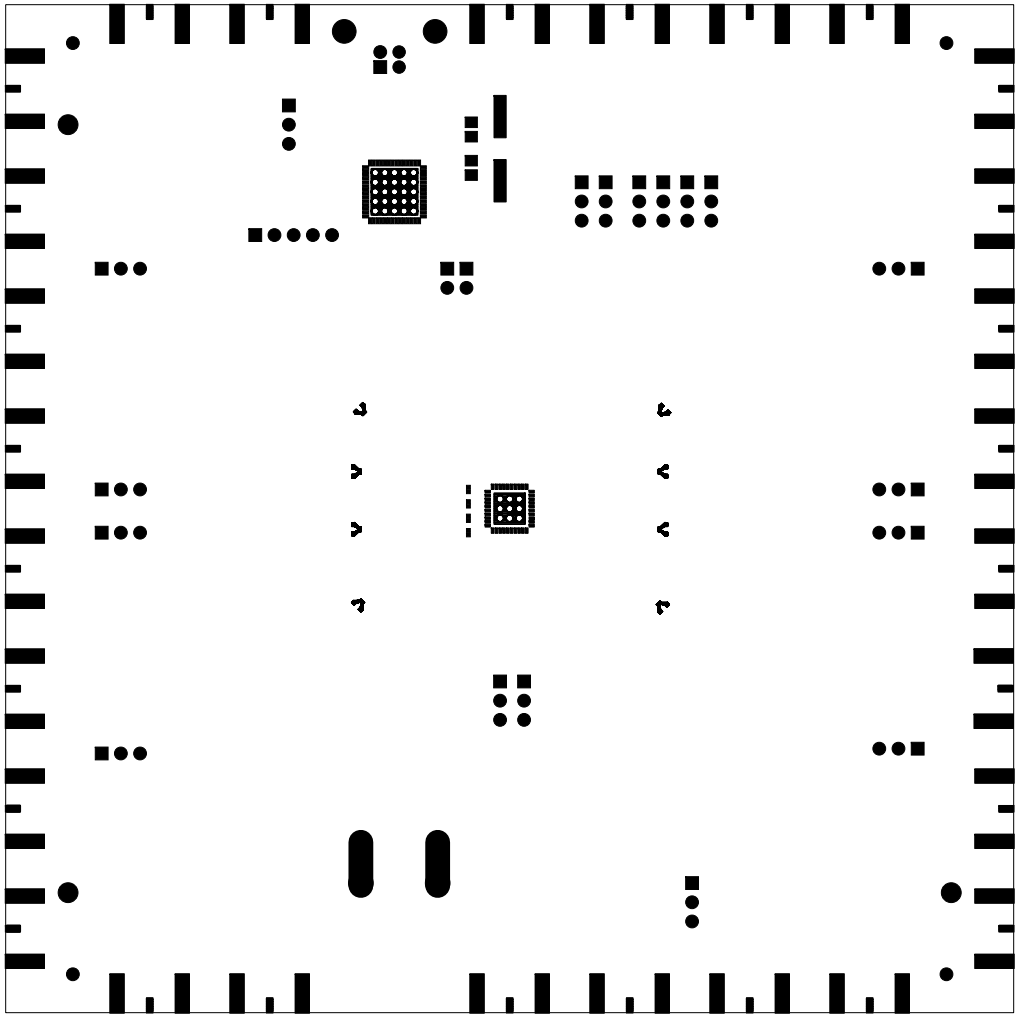
Note: This document is considered uncontrolled unless stamped otherwise.



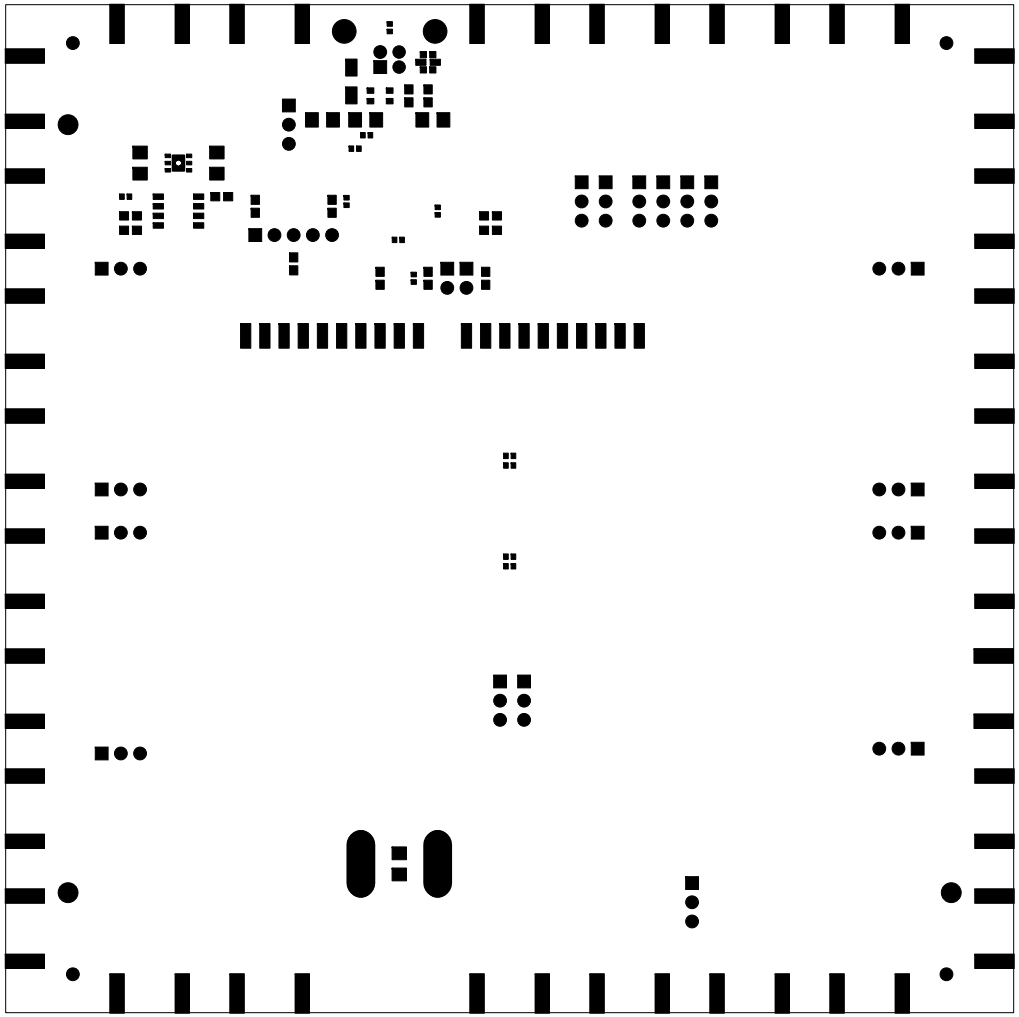
Note: This document is considered uncontrolled unless stamped otherwise.



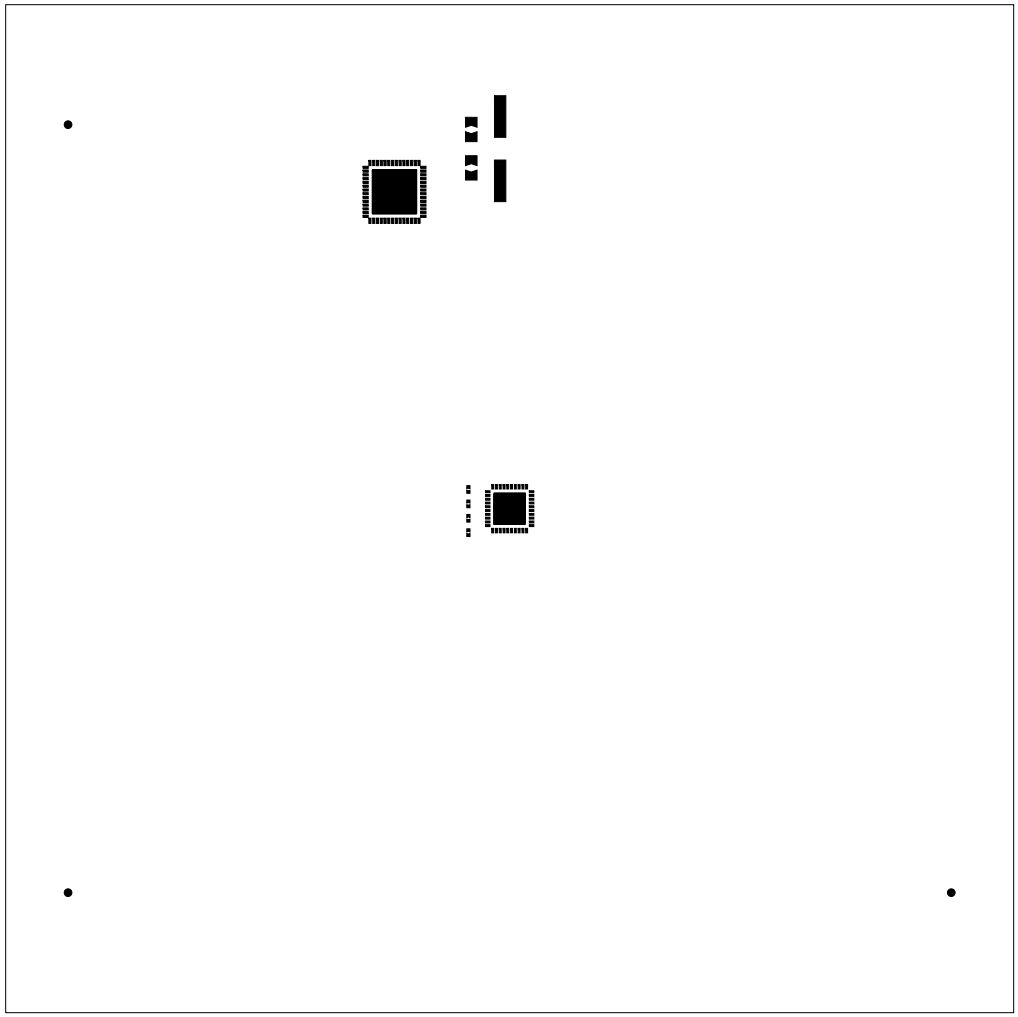
Note: This document is considered uncontrolled unless stamped otherwise.



Note: This document is considered uncontrolled unless stamped otherwise.



Note: This document is considered uncontrolled unless stamped otherwise.



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